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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,792	01/03/2002	Ikuya Oono	XA-9597	8540

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EXAMINER	
CAI, WAYNE HUU	

ART UNIT	PAPER NUMBER
2681	3

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,792	OONO ET AL.	
	Examiner	Art Unit	
	Wayne Cai	2681	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10* is/are allowed.

6)☒ Claim(s) *1 and 7-9* is/are rejected.

7)☒ Claim(s) *2-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al (US – 6,498,927 B2) in view of Bandeira et al (US – 6,728,514 B2).

Regarding claim 1, Kang discloses a signal processing semiconductor integrated circuit device, comprising:

A reception-system circuit including:

- A first amplifier circuit which amplifies a received signal (figure 8, reference number 810)
- Frequency converting means which combines the amplified signal with an oscillation signal having a predetermined frequency to thereby effect frequency conversion on the combined signal (figure 8, reference number 816)
- A second amplifier circuit which is DC coupled to the frequency converting means and amplifies the signal frequency-converted by the frequency converting means (figure 8, reference numbers 830, 846, and 862).

Kang does not disclose the signal processing semiconductor integrated circuit device having a first operation mode in which the reception-system circuit is activated and a second operation mode in which the reception-system circuit is deactivated; wherein voltage reference circuits which respectively generates bias voltages for current sources for supplying operating currents for the frequency converting means and the second amplifier circuit, are activated in response to the transition from the second operation mode to the first operation mode, and thereafter the bias voltages are transferred to the current sources of the frequency converting means and the second amplifier circuit to thereby activate the frequency converting means and the second amplifier circuit.

Bandeira discloses the signal processing semiconductor integrated circuit device having a first operation mode in which the reception-system circuit is activated and a second operation mode in which the reception-system circuit is deactivated (column 12, lines 57-67). However, it is well known in the art that there are at least two (2) operation modes in a communication system, transmit/receive line.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kang's device with Bandeira's transmit/receive line because a communication system is not completed and operated without having a reception system or transmitting system circuit.

Kang further discloses the voltage reference circuits which generates bias voltage for current sources for supplying operating currents for the frequency converting means and the second amplifier circuit, are activated in response to the transition from the second operation mode to the first operation mode, and thereafter the bias voltages are transferred to the current sources of the frequency converting means and the second amplifier circuit to thereby activate the frequency converting means and the second amplifier circuit (column 8, lines 18-34).

Regarding claim 7, Kang, and Bandeira disclose all the limitations in claim 1. Therefore, the claim is interpreted and rejected for the same reason as set forth in claim 1. In addition, Bandeira also discloses all the limitations (figure 6).

A signal processing semiconductor integrated circuit device, comprising:

- A reception-system circuit according to claim 1 (figure 6).

- A transmission-system circuit including a modulation circuit which modulates a transmit signal, and frequency converting means which combines the modulated signal with an oscillation signal to thereby effect frequency conversion on the combined signal (figure 6, reference numbers 618, 628)
- A control-system circuit which controls the reception-system circuit and the transmission-system circuit (figure 6)
- An oscillation-system circuit which generates an oscillation signal or an oscillation control signal combined by the reception-system circuit and the transmission-system circuit (figure 6, reference number 608, 628).

All of them being formed on a single semiconductor substrate.

Regarding claim 8, Kang, and Bandeira disclose all the limitations in claims 1, and 7. Furthermore, Bandeira discloses a wireless communication system comprising:

- A signal processing semiconductor integrated circuit device according to claim 7; and
- A baseband circuit brought into a semiconductor integrated circuit, which performs signal processing for performing the conversion of a signal outputted from the reception-system circuit to a voice signal and the conversion of the voice signal to the transmit signal, and controls the signal processing semiconductor integrated circuit device wherein a command signal for activating the voltage reference circuit and a command signal for activating the frequency converting means and the second amplifier

circuit are supplied from the baseband circuit to the signal processing semiconductor integrated circuit device (column 13, lines 1-11, and figure 6).

Regarding claim 9, Kang teaches the wireless communication system according to claim 8, wherein the command signal for activating the voltage reference circuit and the command signal for activating the frequency converting means and the second amplifier circuit are supplied from the baseband circuit to the control-system circuit lying within the signal processing semiconductor integrated circuit device (column 8, lines 28-34, and figure 8).

Double Patenting

5. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

6. Claims 1-10 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-10 of copending Application No. 10/033,793. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

7. Claims 1-10 are directed to the same invention as that of claims 1-10 of commonly assigned to Hitachi, Ltd. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

Allowable Subject Matter

8. Claims 2-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claim 10 is allowed. Prior art has not been found that suggests or renders obvious the circuit detail of the signal processing semiconductor integrated circuit device disclosed in independent claim 10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wayne Cai whose telephone number is (703) 305-0265. The examiner can normally be reached on Monday-Friday, 10:00-7:30, alternating Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (703) 308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wayne Cai 7/20/04

Wayne Cai
Examiner
Art Unit 2681

WHC

ERIKA GARY
PATENT EXAMINER